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B033312(033)

B. Tech. (Third Semester) Examination, Nov.-Dec. 2020

(New Scheme)

(Information Technology Engg. Branch)

COMPUTER ARCHITECTURE, ORGANIZATION and MICROPROCESSOR

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : *Part (a) is compulsory in each unit and carries 4 marks. Attempt any two parts from (b), (c) and (d) which carry 8 marks each.*

Unit-I

1. (a) Explain the 6 stage at instruction pipeline?

   (b) Explain Micro Programmed Control Unit Organization with proper diagram with working of

Micro Program Sequencer.

(c) Describe the different addressing mode in computer architecture with suitable example.

(d) Explain the need of stack in architecture. How register stack and memory stack execute its operation.

Unit-II

2. (a) What do you mean by divide overflow condition with suitable example.

(b) Draw & explain flow chart of addition & substraction of two fixed point signed magnitude binary number.

(c) Multiply the signed numbers by using Booth's Algorithm (–32)* (64).

(d) Explain Floating Point Division Algorithm with proper example.

Unit-III

3. (a) Write a program whether string "CSVTU" is a palindrome or not explain with flow chart.

(b) Write a program to arrange given series of hexadecimal bytes in ascending order "53, 25, 19, 02".

(c) Write a program to check number 'Decimal Number - 13' is prime or not. If it is prime store 01 in register DL else store 00.

(d) Write 8086 assembly program to implement these 2 instructions - AAA, DAA.

Unit-IV

4. (a) How a MACRO is defined in 8086.

(b) Write a program to generate a delay of 100 ms using an 8086 system that runs on 10 MHz frequency.

(c) Describe interrupt structure of 8086 microprocessor in detail with interrupt vector table.

(d) Explain stack structure of 8086 microprocessor with diagram.

Unit-V

5. (a) Differentiate between I/O mapped I/O and memory mapped I/O?

(b) A digital computer has a memory unit of 64K* 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words.

(i) How many bits are there in tag, index, block & word fields of the address format.

(ii) How many bits are there in each word of cache & how are the divided into function? Include a valid bit.

(iii) How many blocks can the cache accommodate.

(c) Explain how DMA transfer is accomplished with a neat diagram.

(d) What is associative memory? Explain with the help of block diagram. Also maintain the situation in which associative memory can be effectively utilized.